REMARKS

Traversal of Finality

Applicants respectfully traverse the finality of the rejection.

The examiner has not properly responded to the previous amendment by not responding to Applicants arguments and by presenting a number of misstatements of fact.

The Examiner has Made Several Misstatements about the content of the References

Claim 13, as amended, requires that:

> "a vertical body layer of strained silicon formed on an exposed vertical surface of the SiGe layer within the trench, said exposed vertical surface being recessed transversely from an original trench width, and extending upward substantially at said original trench width from the top surface of the lower contact, "

The examiner has missrepresented the location of the transistor body in the Agahi reference

The examiner has claimed on page 2 of the present action that Agahi discloses the structure claimed in claim 13.

Referring to Figures 5 and 6 and paragraphs [035] and [036] of the present specification, the exposed vertical surface is the surface between epi body layer 134 and layer 30 and the phrase "extending upward substantially at said original trench width" refers to the exposed surface of body layer 134, since that phrase is outside the preceding parenthetical phrase.

Applicants point out that Agahi does not show any structure that corresponds to this limitation. Applicants point out that Figure 7 of Agahi shows a layer of silicon 203 having a vertical surface on which is deposited a layer of epi 222 that is described in Column 4, lines 7 - 8 as "the signal transfer region" Region 222 (the transistor body) is an epitaxial silicon region".

The examiner hsas missrepresented the existence of an overhang under the pad nitride.

There is no overhang of a pad dielectric in Agahi's example to produce the vertical surface being recessed from the original trench width, as required by the amended claims 13 and 19.

Fig. 7 of Agahi, shows that the edge of pad nitride 242 is perfectly in line with the vertical surface of layer 203; so there is no transverse recess, as defined by bracket 122 in Fig. 5 of the present spec.

<u>The Examiner Has Not Met the Burden of Finding a Suggestion to Make the Combination of References Cited</u>

It is well known that the examiner is required to find in the references being combined a suggestion to make the combination.

Agahi shows an epi transistor body 134 of silicon formed on the silicon layer 203, so that there is no strain induced in the transistor body.

Hummler shows a single layer 112 of semiconductor that has no epi transistor body associated with it.

The examiner is required to find a suggestion in the references to make the combination, but has not done so.

The examiner has merely stated that: "Applicants argued that the Agahi and Hummler reference do not disclose a strained silicon layer, whereas with the combination of the references a strained silicon layer is formed."(page 4 of the current action, line 2 of the Responses paragraph). The examiner's response clearly ignores the examiner's obligation to find a suggestion in the references to make the combination.

CLAIMS 14 AND 20

The rejection of claims 14 and 20 under 35 USC 103 is also respectfully traversed.

The foregoing arguments also apply to these claims, since they are dependent. In addition, the Examiner has stated: "The buffer layer (in the Imai reference) is SiGe between the substrate and other SiGe layer to form tensile strain and improve speed (Column 4, lines 48 - 65)".

The preceding statement is yet another misstatement, since buffer layer 12 of Fig. 3D does NOT produce strain in SiGe layer 15. Layer 15 is relaxed (Col. 8, lines 33 - 37).

Applicants point out that the suggestion by the examiner: "to modify the devices of Agahi and Hummler by incorporating the SiGe buffer layer between the substrate (203 in Agahi) and other SiGe layer (the substituted SiGe layer from Hummler, referred to as layer 112 in Hummler) to form tensile strain and improve higher speed as taught by Imai" would not produce the effect that the examiner claims.

The substrate (203 in Agahi) is necessarily a horizontal layer. The semiconductor layer 236 (labelled "P-SI" in the center of Fig. 2B of Agahi) adjacent to the transistor body 222 is also horizontal. The buffer layer suggested by the examiner would therefore be a horizontal layer located above layer 272 and below layer 236 in Fig. 2B of Agahi. That suggested buffer layer may or may not have an influence on horizontal crystal spacing the semiconductor layer 236 above it, but it would not have any influence on the transistor body 222, which is vertical and adjacent to the vertical edge of the semiconductor layer (and therefore depends on the vertical crystal spacing of layer 236).

Thus, the buffer layer suggested by the examiner would have no effect on the operation of the vertical transistor required by the claims and there is no motive to make the combination suggested by the examiner.

Applicants point out that the buffer layer 20 in the present invention is interposed to displace the inevitable crystal defects caused by the difference in atomic structure between the bulk silicon of the substrate 10 and the SiGe layer 30 from the region of the vertical transistor (paragraph 22), so that the SiGe layer 30 is fully relaxed. Therefore since the layer 30 is fully relaxed, the improvement in performance of the transistor comes from the strain that results from the difference in crystal spacing between the fully relaxed SiGe layer 30 and the strained vertical silicon transistor body 134.

This is totally different from the operation of the reference as described by the Examiner (page 4 last two lines of the paragraph above 'Response to Arguments'), where the buffer layer causes strain in the transistor body and improves speed.

Response to Arguments

The first response by the examiner relative to the combination of Agahi and Hummler has been dealt with above.

The examiner's response: "In regards to the argument about the silicon layer not being recessed from the original trench width - - " constitutes another misstatement of fact.

The examiner has stated "the silicon layer is under the trench width and is not aligned with the pad nitride (242) and the layer (203)". Fig. 2B of Agahi proves that the examiner's statement is incorrect. Pad nitride 242 is in fact lined up with the right hand edge of P-SI 236 which forms the outer boundary 212 of transistor body 222. The same line continues downward in the Figure into substrate 203.

That right hand edge of P-SI 236 is the counterpart to the exposed vertical surface specified in claim 13. It is evidently NOT recessed from the original trench width because it is aligned with the original trench width. The transistor body 222 of Agahi thus projects into the trench, in contrast

to the requirement in the claims that the transistor body extends upward at the original trench width. Figs 5 and 6 of the present spec illustrate the situation described by the claims. In FIG. 5, the exposed vertical surface of layer 30 is recessed transversely by distance 122 from the original trench width. In FIG. 6, the inner edge of transistor body 134 is aligned with the original trench width.

The examiner's response to the arguments with respect to the Imai reference has been dealt with above. Summarizing, the structure of Imai is incompatible with the structure of the other references, in that the buffer layer of Imai does not (and would not) have any effect on a vertical transistor.

For the foregoing reasons, allowance of the claims is respectfully solicited.

Respectfully submitted,

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